

README

FPGA Design Flow Workshop

The purpose of this workshop is to introduce you to the FPGA design flow using the ISE Foundation software, and is intended for University faculty who are new to Programmable Logic. During the course of the workshop, you will step through the complete Xilinx design flow from design entry to download. The workshop includes slides and labs to help guide you through the flow. The design used in the lab examples throughout the workshop makes use of the 8-bit PicoBlaze controller, which is used to illustrate how to take advantage of various board components.

Required Materials

- **Software**
 - v8.2i ISE Software (see XUP donation request form)
 - v8.2 Chipscope-Pro (see XUP donation request form)
- **Hardware**
 - XUP Virtex-II Pro including download cable and power supply (see XUP donation request form)
 - RS-232 Serial Cable for debug

Prerequisites

- Understanding of basic digital design
- Basic understanding of computer architecture and assembler
- Knowledge of VHDL or Verilog
- Knowledge of assembly language

Directory Structure

The workshop materials should be installed on your PC as follows:

C:/xup/fpgaflow/

- **KCPSM3/Assembler** (directory containing PicoBlaze assembler and template files)
- **KCPSM3/Docs** (directory containing user guides and user manuals for PicoBlaze)
- **KCPSM3/JTAG_loader** (utility for downloading assembled program to FPGA memory – not used for workshop)
- **KCPSM3/Verilog** (directory containing Verilog source code for PicoBlaze and reference designs)
- **KCPSM3/VHDL** (directory containing VHDL source code for PicoBlaze and reference designs)
- **slides** (Power-Point slides used for days 1 and 2)
- **xupv2pro/docs** (directory contains XUP Virtex-II Pro user guide)
- **xupv2pro/labdocs** (contains 6 lab exercises, targeting XUP Virtex-II Pro)
- **xupv2pro/labs/** (contains 6 user lab files, VHDL and Verilog, targeting XUP Virtex-II Pro)
- **xupv2pro/labsolutions/** (contains 6 lab solutions, VHDL and Verilog, targeting XUP Virtex-II Pro)

Day 1 Flow

Presentations (.ppt)	Lab Exercises (.doc)	Lab Files (VHDL and Verilog)
01course_agenda_8		
11_basic_fpga_arch_8		
12_xilinx_tool_flow_8		
12a_tool_flow_lab_intro_8	01_tool_flow_demo_8	Lab1
13_archwiz_and_pace_8		
13a_archwiz_and_pace_lab_intro_8	02_arwz_pace_demo_8	Lab2
14_reading_reports_8		
15_global_time_const_8		
15a_global_time_const_lab_intro_8	03_global_time_const_8	Lab3
16_fpgaDsgnTech_71		

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Day 2 Flow

Presentations (.ppt)	Lab Exercises (.doc)	Lab Files (VHDL and Verilog)
21synch_des_tech_8		
22_floorplanner_adv_8		
23_synthesis_8		
23a_synthesis_lab_intro_8	04_Synthesis_lab_XST_8	Lab4
24_impl_options_8		
25_coregen_8		
25a_coregen_lab_intro_8	05_coregen_lab_8	Lab5
26_chipscope_pro_8		
26a_chipscope_pro_lab_intro_8	06_chipscope_lab_8	Lab6

Lab Overview

Provided with the workshop is the PicoBlaze distribution, which is a free download from the Xilinx web site. The distribution is provided in the KCPSM3 directory and includes the following deliverables:

- Source code (VHDL and Verilog)
- Reference design and HDL testbench
- Assembler and template files

The labs in this design make use of the PicoBlaze 8-bit micro-controller reference design provided with the PicoBlaze distribution, as well as course material developed by Instructor Eric Crabill (Thanks Eric!) from San Jose State University.

Note: If these materials are used in course work, do not distribute or post the solutions on a web site to enable access to students.

The labs are targeted to two boards: XUP Virtex-II Pro and Spartan-3E starter kit. Documentation has been provided, which you will during the course of the workshop to look up information such as pinouts.

Lab Description

Lab Document	Description
01_tool_flow_demo_8	Introduction to ISE flow and picoblaze; use iSIM to simulate design
02_arwz_pace_demo_8	Use architecture wizard to configure and instantiate a Digital Clock manager into a PicoBlaze design. Assign pin locations with PACE. Implement design to generate a bitstream file. Download and test in hardware using hyperterminal.
03_global_time_const_8	Enter and analyze the effects of global timing constraints on a simple PicoBlaze design. Download and test the design in hardware using hyperterminal.
04_Synthesis_lab_XST_8	Set various synthesis options to improve results for a simple PicoBlaze design. Download the design and test in hardware using hyperterminal.
05_coregen_lab_8	Generate the instruction ROM for a PicoBlaze design using CoreGen, initialized with instructions generated from the PicoBlaze assembler. Download and test in hardware.
06_chipscope_lab_8	Use Chipscope-Pro to debug a simple PicoBlaze design using an ILA core.